REMARKS

In response to the above-identified Office Action, Applicant seeks reconsideration thereof. In this response, Applicant does not amend, cancel or add any new claims. Accordingly, claims 8-10, 13-17 and 20-21 are pending.

I. Claims Rejected Under 35 U.S.C. §103(a)

The Patent Office rejects claims 8-10, 14-17 and 21 under 35 U.S.C. 103(a) as being obvious over U.S. Patent No. 4,015,281 issued to Nagata et al. ("Nagata") in view of U.S. Patent No. 5,990,516 issued to Momose et al. ("Momose") and U.S. Patent No. 5,621,681 issued to Moon (Moon"). Applicant respectfully traverses the rejection.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. See MPEP § 2143.

Regarding claim 8, among other elements, claim 8 includes a transistor device comprising a first and second dielectric material being scalable for a set of feature size technologies, the set of feature size technologies defined by a gate length in the range of 25-70 nm. In making the rejection, the Patent Office admits Nagata fails to teach or suggest a set of feature size technologies defined by a gate length in the range of 25-125 nm. See Paper No. 27, page 3. The Patent Office relies in Momose to cure the defects of Nagata.

The Patent Office characterizes Momose as showing "a semiconductor device having double layer gate dielectric in which the feature size technology has a gate length of 150 nm (or 0.15 μm) to form a high performance semiconductor having low power consumption." Paper No. 27, page 3 (citing Momose, col. 16, lines 28-48 and col. 16, line 66 through col. 17, line 32). The Patent Office further characterizes Momose as showing that the gate length can be decreased even more to improve the current drive capability and in one embodiment had a length of 40 nm. See

Paper No. 27, page 3 (citing Momose, col. 15, lines 13-31). Applicant respectfully submits that there is no motivation to combine the teachings of Momose with Nagata.

Momose teaches a semiconductor device comprising a P-type semiconductor substrate having an insulating film, a gate electrode formed on the substrate via the insulating film, and an N-type source/drain region formed on both sides of a channel forming region located under the gate electrode formed on the substrate. Momose, Abstract. Momose discloses the layers are comprised of silicon oxide, silicon nitride, silicon nitric oxide, stacks of silicon nitride and silicon oxide, and laminated layers of tantalum oxide, titanium oxide, strontium and its silicon oxide or silicon nitride films. See Momose, col. 16, line 66 – col. 17, line 11.

The Patent Office relies on Col. 15, lines 13-31 of Momose to teach a gate length 40 nm. See Paper No. 27, page 3. However, in the next paragraph (Col. 15, lines 32-35) Momose states:

> Accordingly, the fore-mentioned transconductance and current drive capability cannot be realized by the conventional method so far reported, and can be realized in accordance with **only** the structure defined by the present invention (emphasis added).

Thus, Applicant respectfully submits Momose teaches that methods prior to Momose do provide a structure suitable for producing a gate length of 40 nm since only the structure defined in Momose was capable of producing such gate lengths. Therefore, one skilled in the art would not be motivated to look to references teaching semiconductor structures that pre-date Momose to combine with Momose to construct a gate with a length of 40 nm. Thus, the proper motivation to combine Momose with Nagata is lacking since Nagata pre-dates Momose and, according to Momose, every structure prior to the structure disclosed in Momose is unsuitable for gate lengths of 40 nm.

In addition, MPEP § 2143.01 under the heading, **FACT THAT REFERENCES CAN BE COMBINED OR MODIFIED IS NOT SUFFICIENT TO ESTABLISH *PRIMA FACIE* OBVIOUSNESS**, states, "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." As stated above, Momose clearly does not suggest it would be desirable to combine Momose with Nagata since Nagata pre-dates Momose. In fact, Momose discourages combination

with any reference that pre-dates Momose since a 40 nm gate length "cannot be realized by the conventional method so far reported...." Momose, Col. 15, lines 32-33.

Moreover, Applicant respectfully submits Momose teaches away from Nagata since the object of Momose is to teach a structure different from structures that pre-date Momose (hence, Momose's insistence on **only** using the structure taught in Momose, which includes elements not included in Nagata), while the Patent Office is suggesting that Momose's teaching can be combined with a structure that pre-dates Momose. Therefore, for at least the above reasons, there is no motivation to combine the teachings of Momose with the teachings of Nagata.

The Patent Office also relies on Moon to cure the defects of Nagata. However, the Patent Office does not cite Moon as teaching or suggesting a transistor device comprising a first and second dielectric material being scalable for a set of feature size technologies, the set of feature size technologies defined by a gate length in the range of 25-70 nm. In addition, in reviewing Moon, Applicant is unable any sections that teach or suggest at least these elements. Therefore, Moon fails to cure the defects of Nagata and Momose.

The failure of the combination of Nagata, Momose and Moon to teach or suggest each of the elements of claim 8 is fatal to the obviousness rejection. Therefore, claim 8 is not obvious over Nagata in view of Momose and Moon. Accordingly, Applicant respectfully requests withdrawal of the rejection of independent claim 8.

Claims 9-10 and 13-14 each depend from claim 8 and contain all of the limitations thereof. Therefore, claims 9-10 and 13-14 are not obvious at least for the same reasons as claim 8. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 9-10 and 13-14.

Regarding the rejection of claim 15, among other elements, claim 15 defines a transistor device comprising a first and second dielectric material being scalable for a set of feature size technologies, the set of feature size technologies defined by a gate length in the range of 25-70 nm similar to claim 8. Therefore, the discussion above regarding the combination of Nagata, Momose and Moon failing to teach or suggest a transistor device comprising a first and second dielectric material being scalable for a set of feature size technologies, the set of feature size technologies

defined by a gate length in the range of 25-70 nm is equally applicable to a similar limitation defined in claim 15. Therefore, claim 15 is not obvious over Nagata in view of Momose and Moon. Accordingly, Applicant respectfully request withdrawal of the rejection of claim 15.

Claims 16-17 and 20-21 depend from claim 15 and contain all of the limitations thereof. Therefore, claims 16-17 and 20-21 are not obvious over Nagata in view of Momose and Moon at least for the same reasons as claim 15. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 16-17 and 20-21.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Patent Office believes that a telephone conference would be useful in moving the application forward to allowance, the Patent Office is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: 12/30/03

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 12/30/03

Nadya Gordon 12/30/03
Nadya Gordon *Date*